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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/620,635	07/16/2003	Myles Kimmitt	2333-US-C	1709

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EXAMINER	
MUL GARY	

ART UNIT	PAPER NUMBER
2416	

MAIL DATE	DELIVERY MODE
04/07/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/620,635	KIMMITT, MYLES	
	Examiner	Art Unit	
	GARY MUI	2416	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 February 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 2* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 2* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Buchanan et al. (US 6,970,435 B1; hereinafter Buchanan) in view of Partyka (US 5,659,580).

For claim 1, Buchanan teaches concurrently generating a plurality of lesser width parallel data words containing parallel data from a greater width parallel data word (see column 2 lines 6 – 15 and column 4 lines 54 – 64; the bit stream is partition into four groups of four bit streams), wherein the number of bits in the greater width parallel data word is greater than the number of bits in each of the lesser width parallel data words (see column 4, lines 55 – 56); serializing parallel data representative of the plurality of lesser width parallel data words (see column 4, lines 62 – 64); and transmitting the serialized data words over a corresponding plurality of distinct serial data channels (see column 5, lines 16 – 17). Buchanan fails to explicitly teach interleaving bits of the greater width parallel data word across the lesser width parallel data

words such that each successive bit of the greater width parallel word is contained within a different one of the lesser width parallel data words. Partyka from the same field of endeavor teaches the interleaving process reorders the data bits such that successive data bits are spread throughout the data block (see column 3 lines 55 – 61). Therefore, it would have been obvious to one skilled in the art at the time of the invention was made to interleave the data as taught by Partyka and then have Buchanan partition the bit stream. The motivation for doing this is to increase the reliability of the system by allow the increasing the ability to correct bit errors.

Claim Rejections - 35 USC § 103

4. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Buchanan et al. (US 6,970,435 B1; hereinafter Buchanan) in view of Partyka (US 5,659,580) and further in view of Nishida et al. (US 5,978,486; hereinafter "Nishida").

For claim 2, Buchanan teaches concurrently generating a plurality of lesser width parallel data words containing parallel data from a greater width parallel data word (see column 2 lines 6 – 15 and column 4 lines 54 – 64; the bit stream is partition into four groups of four bit streams), wherein the number of bits in the greater width parallel data word is greater than the number of bits in each of the lesser width parallel data words (see column 4, lines 55 – 56); serializing parallel data representative of the plurality of lesser width parallel data words (see column 4, lines 62 – 64); and transmitting the serialized data words over a corresponding plurality of distinct serial data channels (see column 5, lines 16 – 17). Buchanan fails to explicitly teach interleaving bits of the greater width parallel data word across the lesser width parallel data

words such that each successive bit of the greater width parallel word is contained within a different one of the lesser width parallel data words. Partyka from the same field of endeavor teaches the interleaving process reorders the data bits such that successive data bits are spread throughout the data block (see column 3 lines 55 – 61). Therefore, it would have been obvious to one skilled in the art at the time of the invention was made to interleave the data as taught by Partyka and then have Buchanan partition the bit stream. The motivation for doing this is to increase the reliability of the system by allow the increasing the ability to correct bit errors. Buchanan fails to disclose scrambling the parallel data in the lesser width parallel data words to form a plurality of scrambled data words. Nishida from the same or similar field of endeavors teach scrambling the parallel data in the lesser width parallel data words to form a plurality of scrambled data words (see column 18, lines 33 – 36). Thus, it would have been obvious to a person of ordinary skill in the art at the time of invention to use scrambling the parallel data in the lesser width parallel data words to form a plurality of scrambled data words in the method taught by Buchanan in order to allow easy clock recovery by averaging changes in amplitude, polarity, and phase of a transmitted signal (see column 1, lines 26 – 29).

Response to Arguments

5. Applicant's arguments filed February 18, 2009 have been fully considered but they are not persuasive.

In response to the remarks, in particular that the references fails to teach interleaving bits of the greater width parallel data word across the less width parallel data words such that each successive bit of said greater with parallel data word is contained within a different on of said

less width parallel data words. The examiner respectfully disagrees. In the Buchanan reference it teaches the partitioning of a 16-bit parallel data stream to four groups of four bits (a nibble) streams (see column 4 line 54 – 56; the generation of lesser width parallel data words from a greater with parallel data word). The four groups are labeled DATAIN0, DATAIN1, DATAIN2, and DATAIN3 contains a nibble of the whole 16-bit parallel data (see column 5 line 19 – 21; adjacent bits of said greater parallel data word contained in different ones of said lesser width parallel words). The nibbles will then be serialized and transmitted on separate serial lines (see column 5 line 15 – 17). However, the Buchanan reference does not explicitly teach interleaving bits of the greater width parallel data word across the less width parallel data words such that each successive bit of said greater with parallel data word is contained within a different on of said less width parallel data words. Partyka from the same field of endeavor teaches the interleaving process reorders the data bits such that successive data bits are spread throughout the data block (see column 3 lines 55 – 61; the data block is interleaved). Therefore, taking the interleaver as taught by Partyka and placing it into Buchanan's system of portioning of bits form the parallel interface into a smaller number of parallel bit streams, where the interleaver of Partyka will interleave the nibbles. Therefore, the claim 1 is rejectable under Buchanan in view of Partyka. For claim 2, it is shown above the combination of Buchanan and Partyka read on the claims and thus claim 2 is rejectable under Buchanan and Partyka in view of Nishaida.

Conclusion

6. **Examiner's Note**: Examiner has cited particular paragraphs or columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

In the case of amending the claimed invention, Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on for proper interpretation and also to verify and ascertain the metes and bounds of the claimed invention.

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary Mui whose telephone number is (571) 270-1420. The examiner can normally be reached on Mon. - Thurs. 9 - 3 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on (571) 272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Ricky Ngo/
Supervisory Patent Examiner, Art Unit 2416

/Gary Mui/
Examiner, Art Unit 2416
04/02/2009